REMARKS

In the Official Action mailed **November 7, 2001**, the Examiner reviewed claims 1-7, 9-16, and 18-20. Claims 1, 2, 7, 10, and 20 were rejected under 35 U.S.C. §102(b), as being anticipated by Dea (USPN 5,469,208, hereinafter "Dea"). Claims 3, 4, 5, and 12 were rejected under 35 U.S.C. 103 (a) as being unpatentable over Dea. Claims 6 and 13-16 were rejected under 35 U.S.C. 103 (a) as being unpatentable over Dea in view of Abramatic et al. (USPN 4,546,383, hereinafter "Abramatic"). Claim 9 was rejected under 35 U.S.C. 103(a) as being unpatentable over Dea in view of Yan (USPN 5,438,374, hereinafter "Yan"). Claim 11 was rejected under 35 U.S.C. 103(a) as being unpatentable over Dea in view of Hardiman (USPN 5,923,223, hereinafter "Hardiman"). Claim 18 was rejected under 35 U.S.C. 103(a) as being unpatentable over the system of Dea and Abramatic as applied to claim 13, and further in view of Yan. Claim 19 was rejected under 35 U.S.C. 103(a) as being unpatentable over the system of Dea and Abramatic as applied to claim 13, and further in view of Hardiman.

Rejections under 35 U.S.C. §102(b) and §103(a)

Independent claim 1 and 20 were rejected as being anticipated by Dea and independent claim 13 was rejected as being unpatentable over Dea in view of Abramatic. Applicant respectfully points out that Dea is directed to a compression/decompression accelerator **coupled to a system bus** (See Dea, Fig. 1). In contrast, the present invention discloses a graphics controller **within a core logic unit** (See Fig. 2, and page 8, lines 4-6 of the instant application). A core logic unit is circuitry within a computer system that interfaces a processor to a memory and a peripheral bus and performs other functions (See page 5, lines 12-13 of the instant application). Specifically, the core logic unit in the present

invention includes the graphics controller and the circuitry of north bridge 118 (see page 8, line 5 of the instant application).

Including the graphics controller into the core logic unit is advantageous because communications between the graphic controller and the core logic elements remain within the core logic unit and are therefore faster than when these communications pass through a system bus. Performing these communications across the system bus is slower because system bus bandwidth is typically less than the bandwidth within the core logic unit, and because of system bus contention with other peripheral devices. There is no suggestion, either explicit or implicit, within Dea, or within Dea in combination with Abramatic, to include the graphics controller within the core logic unit.

In the Official Action mailed **November 7, 2001**, the Examiner states "It is noted the description of the compress/decompression accelerator 120 that includes the function frame difference block 220 at column 6, lines 36-44, and column 5, lines 42-47, and depicted in FIG. 1 and 2, whereas the description at column 5 and Fig. 2 elucidated the compressor/decompressor 120 is a circuitry within the video interface system that interface with the processor 112 to the RAM by way of accelerator bus interface. Therefore, it is considered that description of the compressor/decompressor 120 teaches the claimed apparatus resides inside a core logic chip..."

Applicant respectfully points out that frame difference block 220 of Dea is equivalent to XOR unit 308 (see Dea FIG. 2 and column 6, lines 36-44 and the instant application FIG. 3, and page 9, lines 21-24) and that compression/decompression accelerator 120 of Dea is equivalent to graphics controller 106 of the instant application (see Dea FIG. 1 and column 4, lines 17-19 and the instant application FIG. 2 and page 8, lines 4-6). The remote video processing system 100 of Dea include separate devices, including compression/decompression accelerator 120, to perform the functions of video

processing while the instant application claims graphics controller 106 embedded in a core logic unit such as the north bridge (see Dea FIG.1 and column 4 line 17 to column 5, line 37 and the instant application FIG. 3 and page 8, lines 23-25).

Accordingly, Applicant has amended independent claims 1, 13, and 20 to clarify that the graphics controller is included within the core logic unit such as the north bridge. Dependent claims 8 and 17 were previously cancelled without prejudice.

Hence, Applicant respectfully submits that independent claims 1, 13, and 20 as presently amended are in condition for allowance, and that claims 2-7 and 9-12, which depend upon claim 1, and claims 14-16 and 18-19, which depend on claim 13, are for the same reasons in condition for allowance and for reasons of the unique combinations recited in such claims.

Version with markings to show changes made

The claims:

1. (Twice Amended) An apparatus for compressing video data, comprising:

a video input port, for receiving video data for a current video frame;

a video input buffer coupled to the video input port, for storing video data from the video input port;

a previous frame buffer, for storing at least a portion of a previous video frame;

an operation unit coupled to the video input buffer and the previous frame buffer, for performing an operation between data from the video input buffer and data from the previous frame buffer; and

a result buffer coupled to the operation unit, for storing the result of an operation from the operation unit;

wherein the apparatus resides inside of a north bridge core logic chip for a computer system.

13. (Twice Amended) An apparatus for compressing video data, comprising:

a video input port, for receiving video data for a current video frame;

a video input buffer coupled to the video input port, for storing video data from the video input port;

a previous frame buffer, for storing at least a portion of a previous video frame;

an exclusive-OR unit coupled to the video input buffer and the previous frame buffer, for performing an exclusive-OR operation between data from the video input buffer and data from the previous frame buffer;

a result buffer coupled to the operation unit, for storing the result of an operation from the operation unit;

a memory port coupled to the previous frame buffer and the result buffer, for transferring data to and from a memory that stores video data from the video input port and result data from the result buffer; and

a memory coupled to the memory port for storing the video data from the video input port and result data from the result buffer, wherein the video data is stored to in a current frame in the memory and the result data is stored in a difference frame in the memory;

wherein the apparatus resides inside of a north bridge core logic chip for a computer system.

20. (Twice Amended) A computer system including resources for compressing video, comprising:

a central processing unit within the computer system;

a video input port, for receiving video data for a current video frame;

a video input buffer coupled to the video input port, for storing video data from the video input port;

a previous frame buffer, for storing at least a portion of a previous video frame;

an operation unit coupled to the video input buffer and the previous frame buffer, for performing an operation between data from the video input buffer and data from the previous frame buffer; and

a result buffer coupled to the operation unit, for storing the result of an operation from the operation unit;

wherein the video input port, the video input buffer, the previous frame buffer, the operation unit, and the result buffer reside inside of a north bridge core logic chip for a computer system.

CONCLUSION

It is submitted that the present application is presently in form for allowance. Such action is respectfully requested.

Respectfully submitted,

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